REMARKS

In the above-identified Office Action both of the claims were rejected as being obvious in view of a hypothetical combination of the cited Kuwata and Iwasaki patents. By this response, however, independent Claim 17 has been amended in a manner which is believed to place that claim in condition for allowance over the prior art references.

Particularly, the claimed converter section of Claim 17 requires that input image data having an "a" bit width is converted to data having a bit width of "a" x "2n", where both "a" and "n" are natural numbers. Also, the converted data is required to be temporarily stored in a first FIFO section.

As understood, the Office Action relies on a FIFO2 section of the Kuwata reference as disclosing the above-characterized portion of Applicants' Claim 17. However, referring to lines 44-58 in column 11 of Kuwata, in case of R-pixel data for example, a frame modulation/dither circuit produces R-display data R1 and R2 of two frames each having 1-bit based on an input image data of 6-bits, and stores the data temporarily in FIFO2. Accordingly, a bit width of the image data stored in FIFO2 of Kuwata is 1/6 of the bit width of the input image data, and would be "a" ÷ "2n". This is significantly different from the requirement of Claim 17 of the present invention.

Moreover, according to Kuwata, FIFO2 comprises a register of 40 bits x 3 (120 bits) (see line 61 in column 12 through line 7 in column 13). A data bus width disposed between FIFO2 and DRAM3 is 120 bits (see column 12, lines 28-31). An input into FIFO2 and write and read of DRAM3 are conducted sequentially. Accordingly, the

Kuwata patent does not disclose Applicants' Claim 17 requirement which states that the first FIFO section is of a size suitable for storing image data to full capacity during a time for writing the image data into the frame memory section, reading the data from the frame memory section, and executing a command of that section.

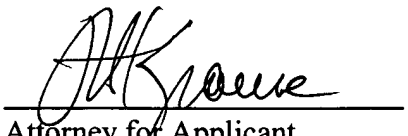
In summary, according to the present invention, by broadening the bit width of the input image data, simultaneously with reading out the image data, writing into the frame memory 1 is conducted at a low speed but is completed in a short period, so as to formulate a free period in which writing into and reading from the frame memory are not conducted, and the free period is used efficiently in executing an active command of the frame memory. On the other hand, an object of Kuwata is that the memory maintenance is conducted so as to shorten the period of writing into and reading from DRAM3 thereby reducing a capacity of the DRAM3, and this object is different from the present invention.

Referring to the cited Iwasaki patent, that reference discloses that an image signal is transferred to a driver 9 at half of a speed of writing into frame memories 4 and 5. However, according to Iwasaki, that writing is conducted at the same speed as an input rate of the input image signal. Thus, Iwasaki differs from the present invention wherein the image data is written into the frame memory at a half rate of the image input rate.

For all of these various reasons Applicants believe that Claims 17 and 18 are allowable, and the issuance of a formal Notice of Allowance is solicited.

Applicant's undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,



Attorney for Applicant
John A. Krause
Registration No. 24,613

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200

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